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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,435	10/11/2001	Bijan Davari	YOR919990101 US2	9650

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EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,435	DAVARI ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 35-56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 35-56 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 51-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 51, lines 7-12, it is unclear how the oxygen ions are implanted so that they pass through the sidewalls of the trench portion to form a buried oxide layer with respect to the sidewalls.

In claim 53, lines 1-4, it is unclear how the trench portion is covered with the first mask to prevent the formation of a buried oxide layer with respect to the sidewalls and bottom of the trench. Also, it is unclear where the buried oxide layer is formed with respect to the sidewalls and the bottom. Also, "said covered trench" has no antecedent basis.

In claim 55, lines 1-3, it is unclear how the ohmic contact are formed to the sidewalls and bottom of the trench. Also, "said covered trench" has no antecedent basis.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 35, 40, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Tadashi Ikeda (JA '323A).

Ikeda teaches a method for forming spaced apart silicon-on-insulator (SOI) regions on a silicon containing substrate 1 comprising the steps (see the English abstract and all figures):

forming a first mask 5 having openings therein on said silicon containing substrate;

implanting oxygen ions 5a through said openings in said first mask into said substrate, wherein the mask blocks the oxygen ions from entering the a bulk region of the substrate, and

after removing the mask, annealing said substrate to form a plurality of first buried oxide regions 3 below a silicon containing layer whereby said spaced apart silicon-on-insulator are formed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 36, 38, 39, 42, 43, 44, 45, 46, and 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tadashi Ikeda (JA '323A) as applied to claims 35, 40, and 41 above, and further in view of Kim (US '652) and Yamazaki (US '846).

Ikeda fails to teach the range for the energy for the implantation of oxygen to obtain the claimed thickness for the buried oxide layers as recited in present claims 36 and 37.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the energy for the implantation of oxygen to obtain the claimed thickness for the buried oxide layers through routine experimentation and optimization to obtain optimal or desired device performance because the range for the energy for the implantation of oxygen to obtain the claimed thickness for the buried oxide layers is a result-effective variable and there is no evidence indicating that the range for the energy for the implantation of oxygen to obtain the claimed thickness for the buried oxide layers is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Ikeda further fails to teach forming the plurality of buried oxide layers as recited in present claims 38 and 39.

Kim teaches a method of forming SOI in which a mask layer 301 having a thickness and an opening is formed on a bulk semiconductor substrate 300, and oxygen is implanted into the semiconductor substrate through the mask layer and opening to form a first buried oxide region and a second buried oxide region, wherein the second buried oxide region is contiguous with the first buried oxide region. See col. 1, line 15 to col. 4, line 30 and all figures.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the plurality of buried oxide layers as taught by Kim in Ikeda's method because in doing so the problem of ESD protection capability is obviated. See col. 1, line 15 to col. 2, line 40.

Ikeda further fails to teach that the mask layer has a slanted edge as recited in present claim 42.

Kim teaches a method of forming SOI in which a mask having a slanted edge during the implantation of oxygen for forming the buried oxide layers. See figure 3B.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use a mask layer having a slanted edge in Ikeda's method because in doing so the problem of ESD protection capability is obviated. See col. 1, line 15 to col. 2, line 40.

Kim fails to teach the range for the angle of the slanted edge of the mask layer as recited in present claim 43.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the angle of slanted edge of the mask layer through routine experimentation and optimization to obtain optimal or desired device performance because for the angle of slanted edge of the mask layer is a result-effective variable and there is no evidence indicating that the range of the angle of slanted edge of the mask layer is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Ikeda further fails to teach that the buried oxide layer is formed by tilted implantation as recited in present claim 44.

However, the use of tilted implantation for forming the buried oxide layer is well-known to one of ordinary skill in the art of making semiconductor devices.

Ikeda further fails to teach the range for the angle of the implantation of oxygen as recited in present claim 45.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the angle of the implantation of oxygen through routine experimentation and optimization to obtain optimal or desired device performance because for the range for the angle of the implantation of oxygen is a result-effective variable and there is no evidence indicating that the range for the angle of the implantation of oxygen is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Ikeda further fails to teach that a field effect transistor is formed in the silicon containing layer as recited in present claim 46.

However, the formation of field effect transistors in a silicon containing layer is well-known to one of ordinary skill in the art of making semiconductor devices.

Ikeda further fails to teach steps of forming trench isolation as recited in present claims 47-50.

Yamazaki teaches a method of forming SOI in which trenches are formed through the SOI regions by removing the silicon substrate and end parts of the buried oxide layer 4' and the trenches are filled with insulator 12. See all figures and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Yamazaki's above teachings into Ikeda's method because in doing so the defects at the boundary between the buried oxide layers and semiconductor substrate are prevented. See col. 3, lines 1-5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Long Pham
Primary Examiner
Art Unit 2814

L.P.
November 7, 2002